REMARKS

Claims 1-85 are currently pending. Applicant reserves the right to pursue original and other claims in this and any other application.

Claims 1-8, 62-65, and 74-77 stand rejected, claims 9-11, 66-68, and 78-80 stand objected to, and claims 12-61, 69-73, and 81-85 are allowed.

Claims 1-8, 62-65, and 74-77 stand rejected under 35 U.S.C. 102(e) as being anticipated by Miyamoto et al. (U.S. Pat. No.6,654,303)("Miyamoto").

Claim 1 recites, *inter alia*, a memory refresh circuit comprising "a control circuit for conducting a memory refresh operation, for monitoring a memory device, and for indicating when said refresh operation is complete based on said monitoring of said memory device."

Miyamoto fails to disclose or suggest "for monitoring a memory device, and for indicating when said refresh operation is complete based on said monitoring of said memory device." The Office mistaken relies on Miyamoto (at Col. 6, lines 48-65) to support the argument that the Miyamoto's monitoring is the same as the claimed invention. At best, Miyamoto relies on a clock signal, and more specifically, a timeout signal to indicate when a memory refresh operation should be done (not when it is done). A refresh operation can take a shorter or longer amount of time than that which was pre-allocated and pre-designated by time period for the time out. This is different from the claimed invention's "monitoring a memory device," which is, as described in the specification as:

> The Refresh Complete outputs of all of the memory devices 530 on lines 551 are in effect logically ORed to provide a signal on line 551 indicating whether any of memory devices 530 is currently performing burst self-refresh, a configuration referred to

> as "wired-OR" or "dynamic OR." Each memory device 530 can selectively couple line 551 to signal ground thus pulling it down from Vdd3. If any of the memory devices 530 couples line 551 to signal ground, then the signal on line 551 received by the power management circuit 550 is at or near signal ground, indicating that a refresh operation is currently underway. If none of the memory devices 530 couple line 551 to ground, resistor 552 pulls down the refresh complete line 551 to the voltage on Vdd3 and the signal on line 551 received by the power management circuit 550 will be approximately Vdd3, indicating that all memory devices 530 have completed their burst self-refresh operation.

(Spec. para. [0028]) As such, Miyamoto is different from the claimed invention for at least that reason. Therefore, the rejection of claim 1 should be withdrawn and the claim allowed.

Claims 2-8 depend, directly or indirectly, from claim1 and are allowable for at least the reason noted above with respect to claim 1.

Claims 62 and 74 have a similar limitation as claim 1 and are allowable for at least the reasons noted above with respect to claim 1.

Claims 63-65 and 75-77 depend, directly or indirectly, from claim 62 and 74, respectively, and are allowable for at least the reason noted above with respect to claim 1.

Claims 9-11, 66-68, and 78-80 stand objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully submits that the base claims are allowable, thus claims 9-11, 66-68, and 78-80 are allowable.

Applicant appreciates the indication of claims 12-61, 69-73, and 81-85 being allowed.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: January 31, 2007

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Michael A. Weinstein
Registration No.: 53,754
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant